A1

In order to solve this problem, a circuit configuration in which image input device 2, processing portions 3 to 6 and image output device 7 are connected in an asynchronous manner, so as to be operated in response to independent clocks, may be considered. Fig. 19 is a block diagram for explaining a circuit configuration in which processing blocks are connected in an asynchronous manner. Referring to Fig. 19, processing blocks A, B and C can operate to perform processing in response to clock signals specific to them.

Replace the paragraph beginning at Page 5, line 30, as follows:

A2

Processing portion 9 performs Log conversion processing for each pixel of the image data input by image input device 8. Processing portion 10 performs MTF correction to data after the Log conversion at processing portion 9. Processing portion 11 performs gamma correction to the data after the MTF correction at processing portion 10. Processing portion 12 binarizes the data after the gamma correction at processing portion 11. The four processings, the Log conversion, MTF correction, gamma correction and binarizing are the same as those previously described. The input processing by the image input device and the output processing by the image output device are the same as those performed by image input device 2 and image output device 7 described above and therefore the description is not repeated.

Replace the paragraph beginning at Page 6, line 16, as follows:

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The data format of image data stored in memory 14 will be now described. Image data consists of a set of a plurality of pieces of pixel data. Referring to Fig. 2, pixel data is

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stored in a format formed of a 3-bit state flag region and a 8-bit data region. A state flag region and a data region for each piece of pixel data will be stored in memory 14.

Replace the paragraph beginning at Page 6, line 28, as follows:

A4

The state flag will be now described. The state flag represents which ones of the processing by processing portions 8 to 13 the pixel data has been through, in other words the flag represents which processing is to be performed next. Fig. 3 is a table for use in illustration of the state flag. The state flag is represented by a 3-digit binary number, in other words by 3 bits. If the state flag is "000", the flag represents that the pixel data stored in the data region is data input by image input device 8 and data which can be subjected to Log conversion by processing portion 9. If the state flag is "001", the flag represents that the pixel data stored in the data region has been subjected to Log conversion, and can be subjected to MTF correction at processing portion 10. Similarly if the state flag is "010", the data has been subjected to MTF correction and can be subjected to gamma correction. If the state flag is "011", the data has been subjected to gamma correction and can be binarized. If the state flag is "110", the data has been binarized and can have its image output. If the state flag is "111", the data has its image output.

Replace the paragraph beginning at Page 9, line 24, as follows:

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In this embodiment image data is stored in memory 14 in the format having the state flag region and data region for each pixel data piece (see Fig. 2), but one state flag may be provided for a plurality of pieces of pixel data, and a format having one state flag

A5

region and a plurality of data regions may be employed. Fig. 8 shows an example of such a format having one state flag region and a plurality of data regions. The format shown in Fig. 8 is effective for example if one state flag is provided for one line of pixel data pieces, or the image data is divided into 3×3 or 5×5 matrices and the pixel data included in each matrix is provided with one flag. If the format shown in Fig. 8 is used, processing portions 9 to 12 each read plural pieces of pixel data for each state of the flag shown in Fig. 8 for executing processing.

Replace the paragraph beginning at Page 10, line 15, as follows:

A6

Referring to Fig. 9, a data processing apparatus according to a second embodiment of the invention includes a state control portion 20 in addition to the construction according to the first embodiment. State control portion 20 is connected to an image input device 8, processing portions 15 to 18, and an image output device 13, and controls these elements. Other than the processings by state control portion 20 and processing portions 15 to 18, the data processing apparatus according to the second embodiment is the same as the data processing apparatus according to the first embodiment, and the description is not repeated here.

Replace the paragraph beginning at Page 11, line 10, as follows:

A7

It is then determined if the final pixel data, in other words, the data which has been read in the end by image input device 8 has the flag "110", and if the flag is "110" (step

A7 S14), the control proceeds to step S15. The control otherwise proceeds to step S11 and the process from steps S11 to S13 is repeated.

Replace the paragraph beginning at Page 11, line 32, as follows:

A8 Once the processing to the read image data has been completed, the processed data is written in memory 14 (step S23). The address to which the data is written at this time is the address received from state control portion 20 in step S20. Once the writing to memory 14 is completed, an end signal is transmitted to state control portion 20 (step S24).

Replace the paragraph beginning at Page 12, line 16, as follows:

A9 Region determining portion 30 determines whether or not pixel data input at image input device 8 is pixel data of a solid image before Log conversion by processing portion 15.

Replace the paragraph beginning at Page 13, line 17, as follows:

A10 Referring to Fig. 14, in the region determining processing, if the data is determined to be solid image data, the state flag is rewritten into "100". The image data having the state flag rewritten into "100" is then subjected to binarizing.

Replace the paragraph beginning at Page 15, line 11, as follows:

A11 The state flag of the data processing apparatus according to the fourth embodiment will be now described. Referring to Fig. 17, if region determining portion 46 determines

A11 that pixel data is solid image data, the state flag is rewritten into "101" and otherwise rewritten into "001".

Replace the paragraph beginning at Page 15, line 15, as follows:

A12 In processing portion 41 to execute color conversion processing, pixel data having a state flag of "001" or "101" is subjected to color conversion. As for pixel data having a state flag of "001", the state flag is rewritten into "010", and as for pixel data having a state flag of "101", the state flag is rewritten into "110" after the completion of the color conversion.

Replace the Abstract appearing on Page 21 as follows:

A13 A data processing system has the following construction in order to reduce the memory capacity and the cost. A plurality of processors perform a series of processings on input image data in a prescribed order, including Log conversion, MTF correction, gamma correction and binarization. A shared memory stores pixel data to be processed, and a state flag is used to represent the state of processing of the data for each pixel in association with each other. Processings by the plurality of processors are executed asynchronously.

IN THE CLAIMS:

Please amend claims 1, 3, 5, 6, 8-13, 15, 16, and 18-20 as follows:

A14 sub A1 1. (Amended) A data processing system comprising: